CLAIMS

What is claimed is:

1. A clock based voltage deviation detector comprising:

a pulse module having a pulse input for receiving a clock signal and a pulse output for outputting a stream of reset pulses;

an indicator module having a first indicator input for receiving an input signal, a second indicator input for receiving a reference voltage, a third indicator input communicatively coupled to said pulse output of said pulse module and an indicator output for outputting a pass/fail indicator signal as a function of said stream of reset pulses and a difference between an input signal and a reference voltage; and

a correlation module having a first correlation input for receiving said clock signal, a second correlation input communicatively coupled to said indicator output of said indicator module, wherein an event of said pass/fail indicator is correlated to a period of said clock signal at which said event occurred.

2. The clock based voltage deviation detector according to Claim 1, wherein said pulse module comprises:

a delay cell having a first delay input for receiving said clock signal and a delay output for outputting a delayed clock signal as a function of said clock signal; and

an exclusive-OR gate having a first exclusive-OR input for receiving said clock signal, a second exclusive-OR input communicatively coupled to said delay output of said delay cell and an exclusive-OR output for outputting said stream of reset pulses as a function of said clock signal and said delayed clock signal.

3. The clock based voltage deviation detector according to Claim 1, wherein said correlation module comprises:

a counter having a counter input for receiving said clock signal and a counter output for outputting a count value as a function of said clock signal; and

a storage module having a first storage input communicatively coupled to said counter output and a second storage input for receiving said pass/fail indicator, wherein said count value corresponding to said event of said paid/fail indicator is stored.

4. The clock based voltage deviation detector according to Claim 1, wherein said indicator module comprises:

a comparator having a first comparator input for receiving said input signal, a second comparator input for receiving said reference voltage and a comparator output for outputting a trip signal as a function of a difference between said input signal and said reference voltage; and

a latch having a first input communicatively coupled to said comparator output of said comparator, a second input communicatively coupled to said pulse output and a latch output for outputting said pass/fail indicator as a function of said trip signal and said stream of reset pulses.

5. The clock based voltage deviation detector according to Claim 1, wherein said indicator module comprises a latch-enabled comparator having a first comparator input for receiving said input signal, a second comparator input for receiving said reference voltage, a

third comparator input communicatively coupled to said pulse output of said pulse module and a comparator output for outputting said pass/fail indicator as a function of said stream of reset pulses and a difference between said input signal and said reference voltage.

6. The clock based voltage deviation detector according to Claim 1, wherein:

said pulse module further has a second pulse output for outputting a stream of delayed reset pulses as a function of said clock signal; and

said indicator module further has a second indicator output for outputting said pass/fail indicator as a function of said delayed stream of reset pulses.

7. The clock based voltage deviation detector according to Claim 6, wherein said pulse module comprises:

a first delay cell having a first delay input for receiving said clock signal and a first delay output for outputting a delayed clock signal as a function of said clock signal;

an exclusive-OR gate having a first exclusive-OR input for receiving said clock signal, a second exclusive-OR input communicatively coupled to said first delay output for outputting said stream of reset pulses as a function of said clock signal and said delayed clock signal; and

a second delay cell having a second delay input communicatively coupled to said exclusive-OR output of said exclusive-OR gate and a second delay output for outputting said stream of delayed reset pulses as a function of said stream of reset pulses.

8. The clock based voltage deviation detector according to Claim 6, wherein said pulse module comprises:

a first delay cell having a first delay input for receiving said clock signal and a first delay output for outputting a first delayed clock signal as a function of said clock signal;

a first exclusive-OR gate having a first exclusive-OR input for receiving said clock signal, a second exclusive-OR input communicatively coupled to said first delay output of said first delay cell and a first exclusive-OR output for outputting said stream of reset pulses as a function of said clock signal and said first delayed clock signal;

a second delay cell having a second delay input for receiving said clock signal and a second delay output for outputting a second delayed clock signal as a function of said clock signal;

a third delay cell having a third delay input communicatively coupled to said second delay output of said second delay cell and a third delay output for outputting a third delayed clock signal as a function of said second delayed clock signal; and

a second exclusive-OR gate having a third exclusive-OR input communicatively coupled to said second delay output of said second delay cell, a fourth exclusive-OR input communicatively coupled to said third delay output of said third delay cell and a second exclusive-OR output for outputting said stream of delayed reset pulses as a function of said second delayed clock signal and said third delayed clock signal.

9. The clock based voltage deviation detector according to Claim 6, wherein said indicator module comprises:

a first latch-enabled comparator having a first comparator input for receiving said input signal, a second comparator input for receiving said reference voltage, a third comparator input communicatively coupled to said pulse output of said pulse module and a first comparator output for outputting a first trip signal as a function of said stream of reset pulses and a difference between said input signal and said reference voltage;

a second latch-enabled comparator having a fourth comparator input for receiving said input signal, a fifth comparator input for receiving said reference voltage, a sixth comparator input communicatively coupled to said second pulse output of said pulse module and a second comparator output for outputting a second trip signal as a function of said stream of delayed reset pulses and said difference between said input signal and said reference voltage; and

a summing circuit having a first summing input communicatively coupled to said first comparator output of said first latch-enabled comparator, a second summing input communicatively coupled to said second comparator output of said second latch-enabled comparator and a first summing output for outputting said pass/fail indicator signal as a function of said first trip signal and said second trip signal.

10. A clock based voltage deviation detector comprising:

a pulse module for generating a stream of reset pulses as a function of a clock signal;

an indicator module for generating a pass/fail indicator signal as a function of said stream of reset pulses and a difference between an input voltage and a reference voltage;

a counter for generating a count value as a function of said clock signal; and

a storage module for saving a particular count value at which an event of said pass/fail signal occurs.

11. The clock based voltage deviation detector according to Claim 10, wherein said pulse module comprises:

an OR gate having an OR gate input for receiving said clock signal; and

an exclusive-OR gate having first input for receiving said clock signal, a second input communicatively coupled to an OR gate output of said OR gate, and an output for outputting said stream of reset pulses.

12. The clock based voltage deviation detector according to Claim 11, wherein said indicator module comprises a latch-enabled comparator having a first comparator input for receiving said input voltage a second comparator input for receiving said reference voltage, a third comparator input for receiving said stream of reset pulses, and a comparator output for outputting said pass/fail indicator signal.

13. The clock based voltage deviation detector according to Claim 12, wherein:

said first comparator input of said latch-enabled comparator comprises a non-inverting input;

said second comparator input of said latch-enabled comparator comprises an inverting input;

said third comparator input of said latch-enabled comparator comprises a latch enable input; and

said event comprises an overvoltage.

14. The clock based voltage deviation detector according to Claim 12, wherein:

said first comparator input of said latch-enabled comparator comprises an inverting input;

said second comparator input of said latch-enabled comparator comprises a non-inverting input;

said third comparator input of said latch-enabled comparator comprises a latch enable input; and

said event comprises an undervoltage.

15. The clock based voltage deviation detector according to Claim 10, wherein:

said pulse module further generates a stream of delayed reset pulses as a function of said clock signal; and

said indicator module further generates said pass/fail indicator as a function of said delayed stream of reset pulses.

16. The clock based voltage deviation detector according to Claim 15, wherein said pulse module comprises:

a first OR gate having a first OR gate input for receiving said clock signal;

a first exclusive-OR gate having a first exclusive-OR gate input for receiving said clock signal, a second exclusive-OR gate input communicatively coupled to a first OR gate

output of said first OR gate, and an exclusive-OR gate output for outputting said stream of reset pulses;

a second OR gate having a second OR gate input for receiving said clock signal;

a third OR gate having a third OR gate input communicatively coupled to a second OR gate output of said second OR gate; and

a second exclusive-OR having a third exclusive-OR gate input communicatively coupled to said second OR gate output of said second OR gate, a fourth exclusive-OR gate input communicatively coupled to a third OR gate output of said third OR gate and a second exclusive-OR gate output for outputting said stream of delayed reset pulses.

17. The clock based voltage deviation detector according to Claim 16, wherein said indicator module comprises:

a first latch-enabled comparator having a first comparator input for receiving said input voltage, a second comparator input for receiving said reference voltage, a third comparator input communicatively coupled to a first NOR gate output of a first NOR gate;

said first NOR gate having a first NOR gate input communicatively coupled to a first inverted output of said first latch-enabled comparator and a second NOR gate input for receiving said stream of reset pulses;

a second latch-enabled comparator having a fourth comparator input for receiving said input voltage, a fifth comparator input for receiving said reference voltage, a sixth comparator input communicatively coupled to a second NOR gate output of a second NOR gate;

said second NOR gate having a third NOR gate input communicatively coupled to a second inverted output of said second latch-enabled comparator and a fourth NOR gate input for receiving said stream of delayed reset pulses; and

a fourth OR gate having a fourth OR gate input communicatively coupled to a first non-inverted output of said first latch-enabled comparator, a fifth OR gate input communicatively coupled to a second non-inverted output of said second latch-enabled comparator and a fourth OR gate output for outputting said pass/fail indicator signal.

18. A clock based voltage deviation detector comprising:

a means for generating a reset pulse stream as a function of a clock signal;

a means for generating a pass/fail indicator signal as a function of said reset pulse stream and an event of a monitored voltage; and

a means for correlating an event of said pass/fail indicator signal with a period of said clock signal at which said event occurred.

19. The clock based voltage deviation detector according to Claim 18, further comprising:

a means for generating a delayed reset pulse stream as a function of said clock signal; and

a means for further generating said pass/fail indicator signal as a function of said delayed clock signal.

20. The clock based voltage deviation detector according to Claim 19, wherein said means for generating a pass/fail indicator signal comprises:

a means for detecting said event of said monitored voltage and generating a first trip signal until receipt of a next pulse of said reset pulse stream;

a means for detecting said event of said monitored voltage and generating a second trip signal until receipt of a next pulse of said delayed reset pulse stream; and

a means for generating said pass/fail indicator signal as a function of said first trip signal and said second trip signal.